

1. Maximum rate single-phase clocking of a closed pipeline including wave pipelining, stoppability, and startability
Chuan-Hua Chang; Davidson, E.S.; Sakallah, K.A.;
[Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on](#)
Volume 14, [Issue 12](#), Dec. 1995 Page(s):1526 - 1545
Digital Object Identifier 10.1109/43.476583

[AbstractPlus](#)

| Full Text:

[PDF\(1820](#)

[KB\)](#) [IEEE](#)

[JNL](#)

[Rights and](#)

[Permissions](#)

2. A Single-Stream Pipelined Instruction Decompression System for Embedded Microprocessors
Yuan-Long Jeang; Tzuu-Shaang Wey; Hung-Yu Wang; Chih-Chung Tai;
[Intelligent Information Hiding and Multimedia Signal Processing, 2006. IHH-MSP '06. International Conference on](#)
Dec. 2006 Page(s):571 - 574
Digital Object Identifier 10.1109/IHH-MSP.2006.265067

[AbstractPlus](#) | Full Text: [PDF\(196 KB\)](#) [IEEE](#) [CNF](#)

[Rights and Permissions](#)

3. A New and Efficient Field-Partition Based Code Compression and Its Pipelined Decompression System
Yuan-Long Jeang; Chih-Chung Tai; Yong-Zong Lin;
[Innovative Computing, Information and Control, 2006. ICICIC '06. First International Conference on](#)
Volume 2, 30-01 Aug. 2006 Page(s):10 - 13
Digital Object Identifier 10.1109/ICICIC.2006.206

[AbstractPlus](#) | Full Text: [PDF\(152 KB\)](#) [IEEE](#) [CNF](#)

[Rights and Permissions](#)

4. Interfacing synchronous and asynchronous modules within a high-speed pipeline
Sjogren, A.E.; Myers, C.J.;
[Very Large Scale Integration \(VLSI\) Systems, IEEE Transactions on](#)
Volume 8, [Issue 5](#), Oct. 2000 Page(s):573 - 583
Digital Object Identifier 10.1109/92.894162

[AbstractPlus](#) | [References](#) | Full Text: [PDF\(176 KB\)](#) [IEEE](#) [JNL](#)

[Rights and Permissions](#)

5. An Efficient Field-Partition Based Code Compression and Its Pipelined Decompression System
Yuan-Long Jeang; Yong-Zong Lin;
[VLSI Design, Automation and Test, 2006 International Symposium on](#)
April 2006 Page(s):1 - 4
Digital Object Identifier 10.1109/VDAT.2006.258133

[AbstractPlus](#) | Full Text: [PDF\(3666 KB\)](#) [IEEE](#) [CNF](#)

[Rights and Permissions](#)

6. Interfacing synchronous and asynchronous modules within a high-speed pipeline
Sjogren, A.E.; Myers, C.J.;
[Advanced Research in VLSI, 1997. Proceedings. Seventeenth Conference on](#)
15-16 Sept. 1997 Page(s):47 - 61
Digital Object Identifier 10.1109/ARVLSI.1997.634845


[AbstractPlus](#) | Full Text: [PDF\(808 KB\)](#) [IEEE](#) [CNF](#)


[Rights and Permissions](#)


7. Exploiting Low Entropy to Reduce Wire Delay
Citron, D.;
[Computer Architecture Letters](#)
Volume 3, [Issue 1](#), Jan. 2004 Page(s):1 - 1
Digital Object Identifier 10.1109/L-CA.2004.7

[AbstractPlus](#) | Full Text: [PDF\(200 KB\)](#) [IEEE](#) [JNL](#)

[Rights and Permissions](#)

-  8. Workload characterization for the design of future servers
Maron, B.; Chen, T.; Vianney, D.; Olszewski, B.; Kunkel, S.; Mericas, A.;
[Workload Characterization Symposium, 2005. Proceedings of the IEEE International](#)
6-8 Oct. 2005 Page(s):129 - 136
Digital Object Identifier 10.1109/IIISWC.2005.1526009

[AbstractPlus](#) | Full Text: [PDF](#)(423 KB) [IEEE CNF](#)
[Rights and Permissions](#)
-  9. Context-aware task assignment in ubiquitous computing environment - A genetic algorithm based approach
Pawar, Pravin; Mei, Hailiang; Widya, Ing; van Beijnum, Bert-Jan; van Halteren, Aart;
[Evolutionary Computation, 2007. CEC 2007. IEEE Congress on](#)
25-28 Sept. 2007 Page(s):2695 - 2702
Digital Object Identifier 10.1109/CEC.2007.4424811

[AbstractPlus](#) | Full Text: [PDF](#)(309 KB) [IEEE CNF](#)
[Rights and Permissions](#)
-  10. A deterministic globally asynchronous locally synchronous microprocessor architecture
Heath, M.; Harris, I.;
[Microprocessor Test and Verification: Common Challenges and Solutions, 2003. Proceedings. 4th International Workshop on](#)
29-30 May 2003 Page(s):119 - 124

[AbstractPlus](#) | Full Text: [PDF](#)(265 KB) [IEEE CNF](#)
[Rights and Permissions](#)